반도체 관련 Soft Error 및 신뢰성 확보 방안

Sep. 26th, 2019

기중식

Electronic Voting Machine in Belgium 2003

- One candidate got 4096 extra votes
- Spontaneous creation of a bit at position 13 in the memory of the computer

Singapore to Perth Qantas A330, 2008

- Un-commanded rapidly descending 210m and 110 passenger injured
- Air data inertial reference unit (ADIRU) erroneously relabeled the altitude data word

목차

Hard Error vs Soft Error

Hard Error

An error induced by faulty device operation. DATA is lost and data an no longer be stored at that location

Soft Error

A random error induced by an event which corrupts the DATA stored in a device. The device itself is not damaged

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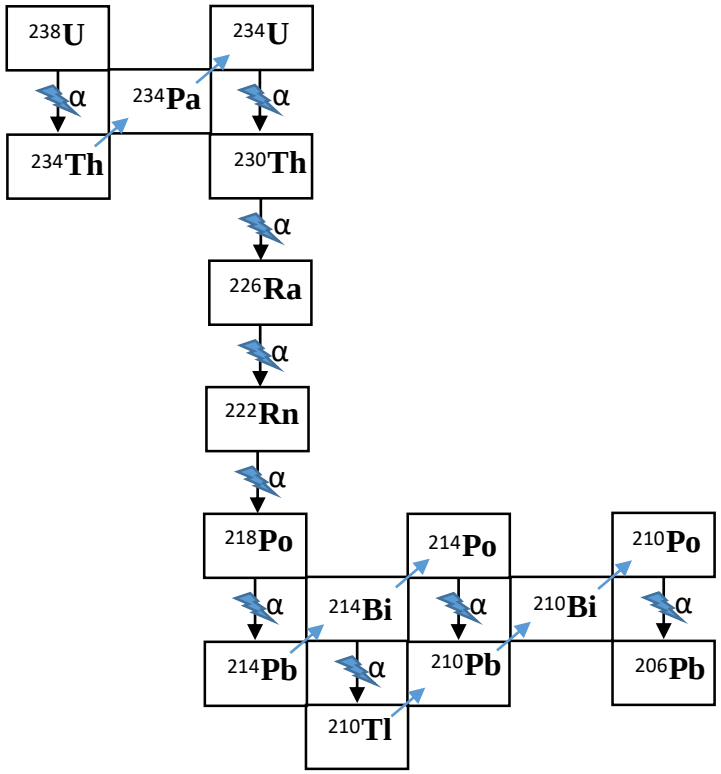
반도체 Soft Error의 발생원과 Mechanism

반도체 Soft Error의 발생원

- Alpha particles from radioactive nuclides in nature
- Neutron from cosmic ray

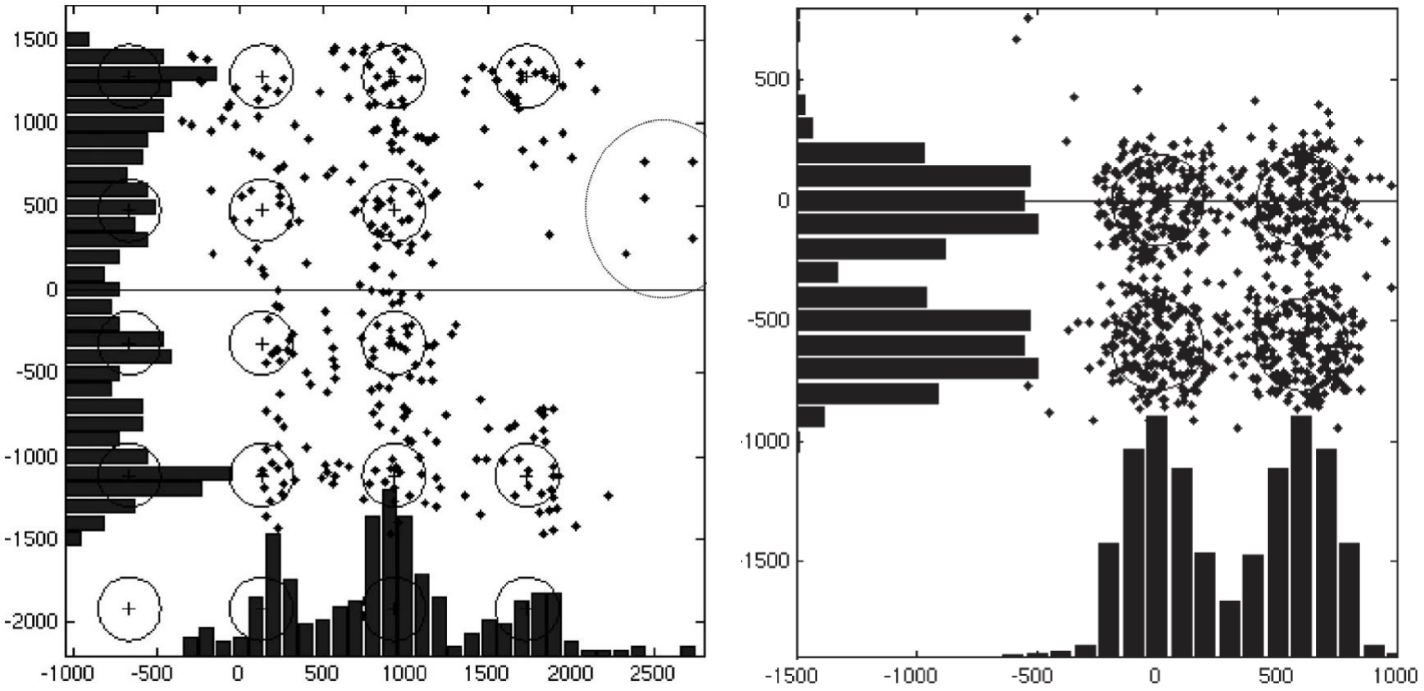
Alpha Particle의 발생

➢Uranium 238 radioactive decay chain



알파 입자가 의료 장비에 미치는 영향

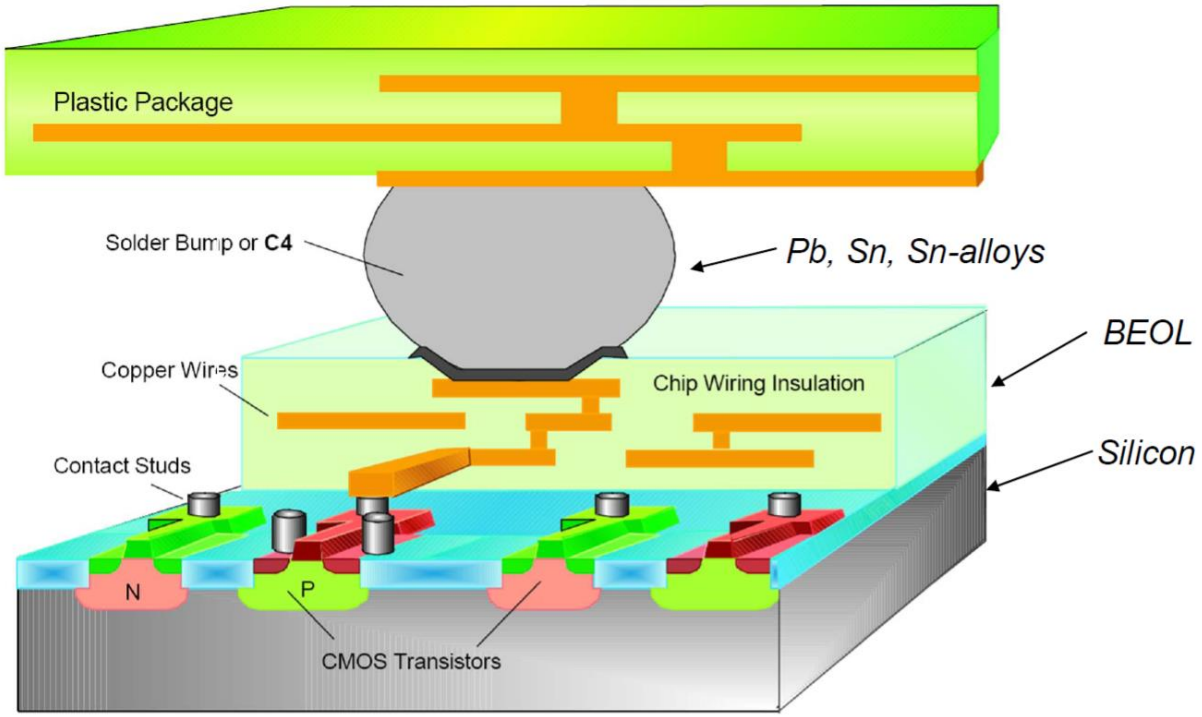
- 맥박 조정기에 연결된 SRAM에서 오류율이 $12X10^6$ FIT/MBit로 증가



Wilkinson, J.D., at al, "A cautionary tale of soft errors induced by SRAM packaging materials," IEEE Trans. Dev. Mat. Reliab., 5 (3)

솔더볼 위치와 소프트 오류가 집중적으로 발생하는 지점이 일치

반도체 패캐지 내부의 알파 입자 요인

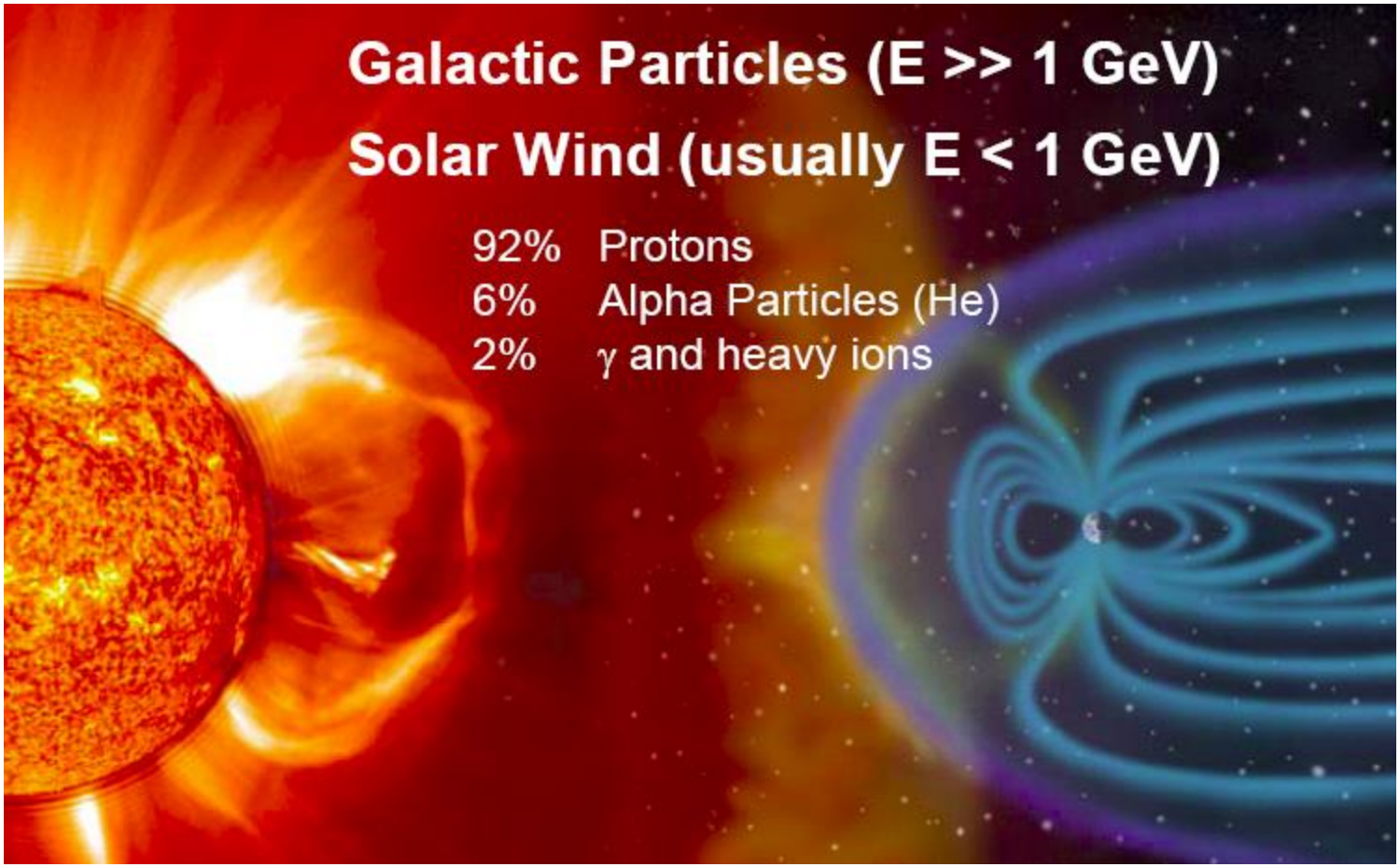


Michael Gordon, "Challenges in Ultra-low Emissivity Alpha Particle Detection", IBM TJ Watson Research Center

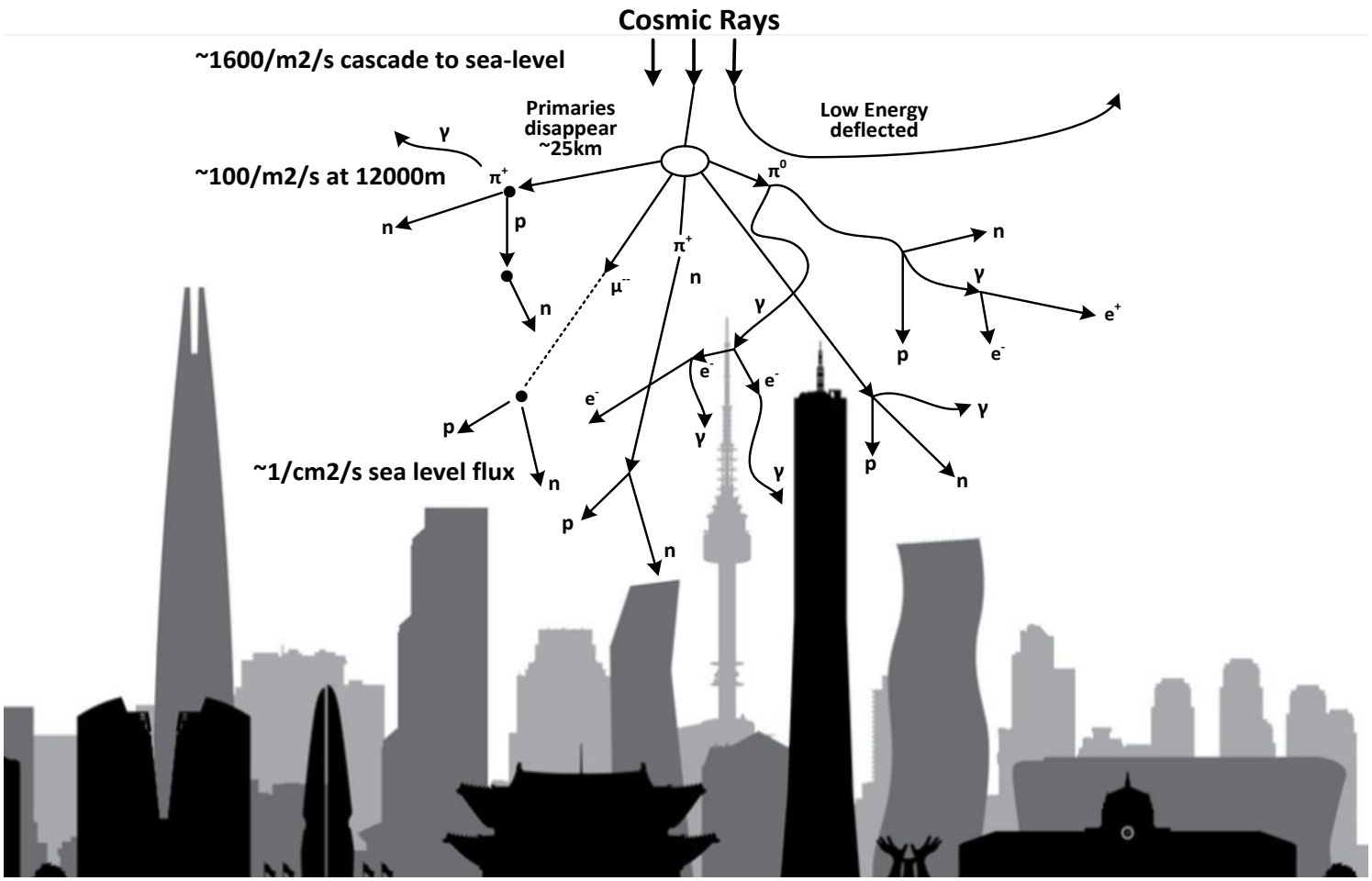
알파 입자 방사량

Material	Alpha radiation Flux (a/khr cm2)
Processed wafers	0.9
Cu metal	1.9
Al metal	1.4
Mold compound	24 to <2
Under-fill	2 to 0.9
Pb solders	7200 to <2
Alloy 42	8

Cosmic Ray

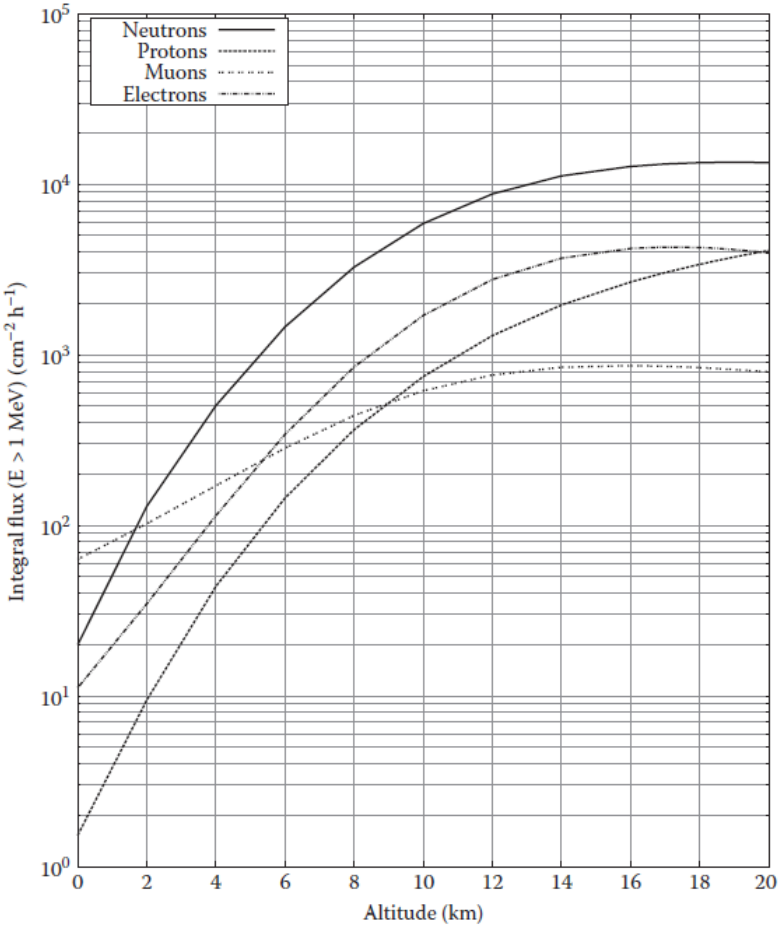

Galactic Particles (E >> 1 GeV)
Solar Wind (usually E < 1 GeV)
92% Protons
6% Alpha Particles (He)
2% γ and heavy ions

대기 중성자의 발생



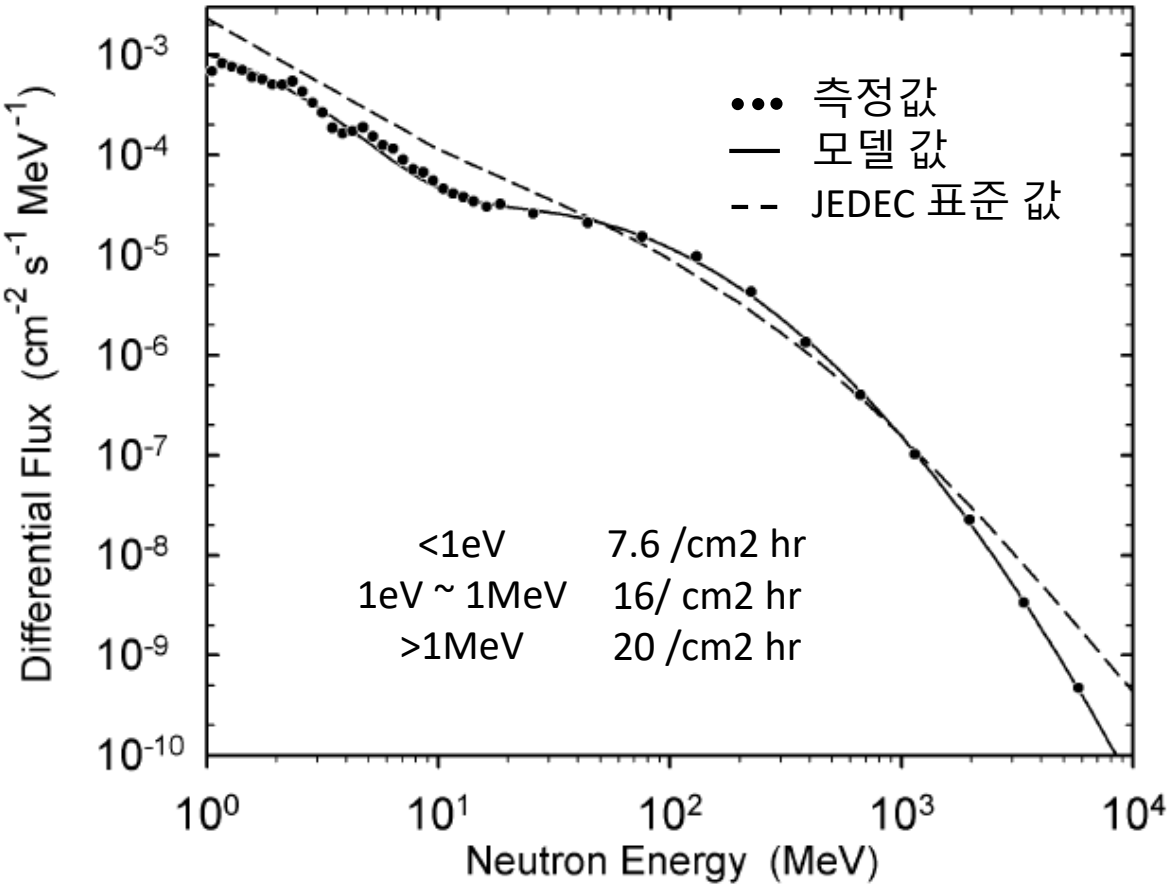
Costenaro, Enrico. "Techniques pour l'évaluation et l'amélioration du comportement des technologies émergentes face aux fautes aléatoires." PhD diss., Grenoble Alpes, 2015.

고도에 따른 대기 입자의 Flux 변화



K. Iniewski, et al, “Soft errors, from particles to circuits”

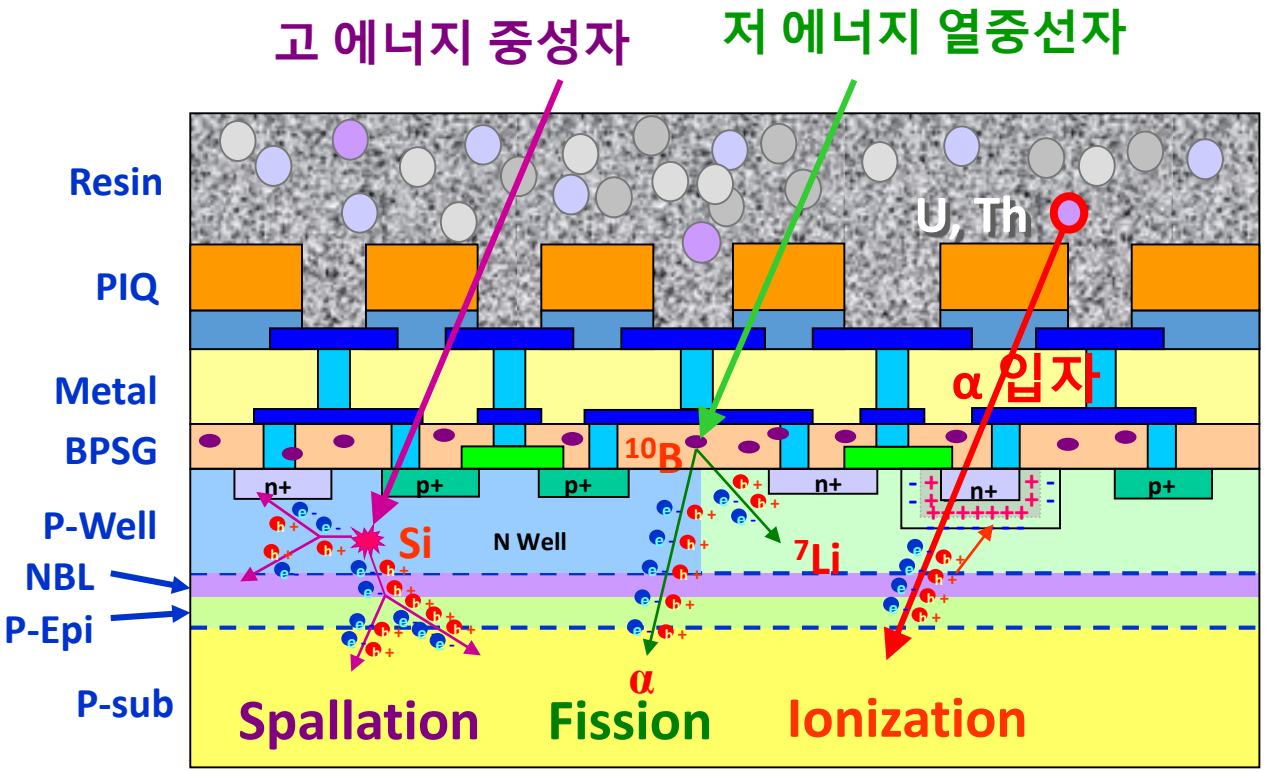
중성자의 에너지 별 Differential Flux



Gordon, M.S. et al, "Measurement of the flux and energy spectrum of cosmic-ray induced neutrons on the ground", Nuclear Science, IEEE Trans , Vol:51 Iss:6, Dec 2004 pp3427 - 3434

Soft Error 발생 Mechanism

➢ Soft Error는 회로 노드에 모여진 총 전하량이 임계 상태 (Qcrit)보다 커서 논리 상태를 뒤집을 때 발생



Soft Error의 종류

SEE Type	Description	Device Affected
Single Event Upset (SEU)	Corruption of the information stored in a memory element	Memories, latches in logic devices
Multiple Bit Upset (MBU)	Several memory elements corrupted by a single strike	Memories, latches in logic devices
Single Event Functional Interrupt (SEFI)	Corruption of a data path leading to loss of normal operation	Complex devices with built-in state machine/control sections
Single Hard Error (SHE)	Unalterable change of state in a memory element	Memories, latches in logic devices
Single Event Transient (SET)	Impulse response of certain amplitude and duration	Analog and Mixed Signal circuits, Photonics
Single Event Disturb (SED)	Momentary corruption of the information stored in a bit	combinational logic, latches in logic devices
Single Event Latchup (SEL)	High-current conditions	CMOS, BiCMOS devices
Single Event Snapback (SESB)	High-current conditions	N-channel MOSFET, SOI devices
Single Event Burnout (SEB)	Destructive burnout due to high-current conditions	BJT, N-channel Power MOSFET
Single Event Gate Rupture (SEGR)	Rupture of gate dielectric due to high electrical field conditions	Power MOSFETs, Non-volatile NMOS structures, VLSIs, linear devices

F. Sturesson "Single Event Effects (SEE) Mechanism and Effects," based on Based on RADECS Short Course 2003 by S.Duzellier

"Soft errors induce the highest failure rate of all other reliability mechanisms combined." Baumann, Robert.

- "The SER of advanced CMOS devices is **higher than all other reliability mechanisms combined.**"

  Baumann, Robert. "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction." IEDM'02.

- "Left unchallenged, **soft errors** have the potential for inducing **the highest failure rate of all other reliability mechanisms combined.**

  Baumann, Robert. "Radiation-induced soft errors in advanced semiconductor technologies." IEEE Trans on Device & materials reliability 5, no. 3 (2005)

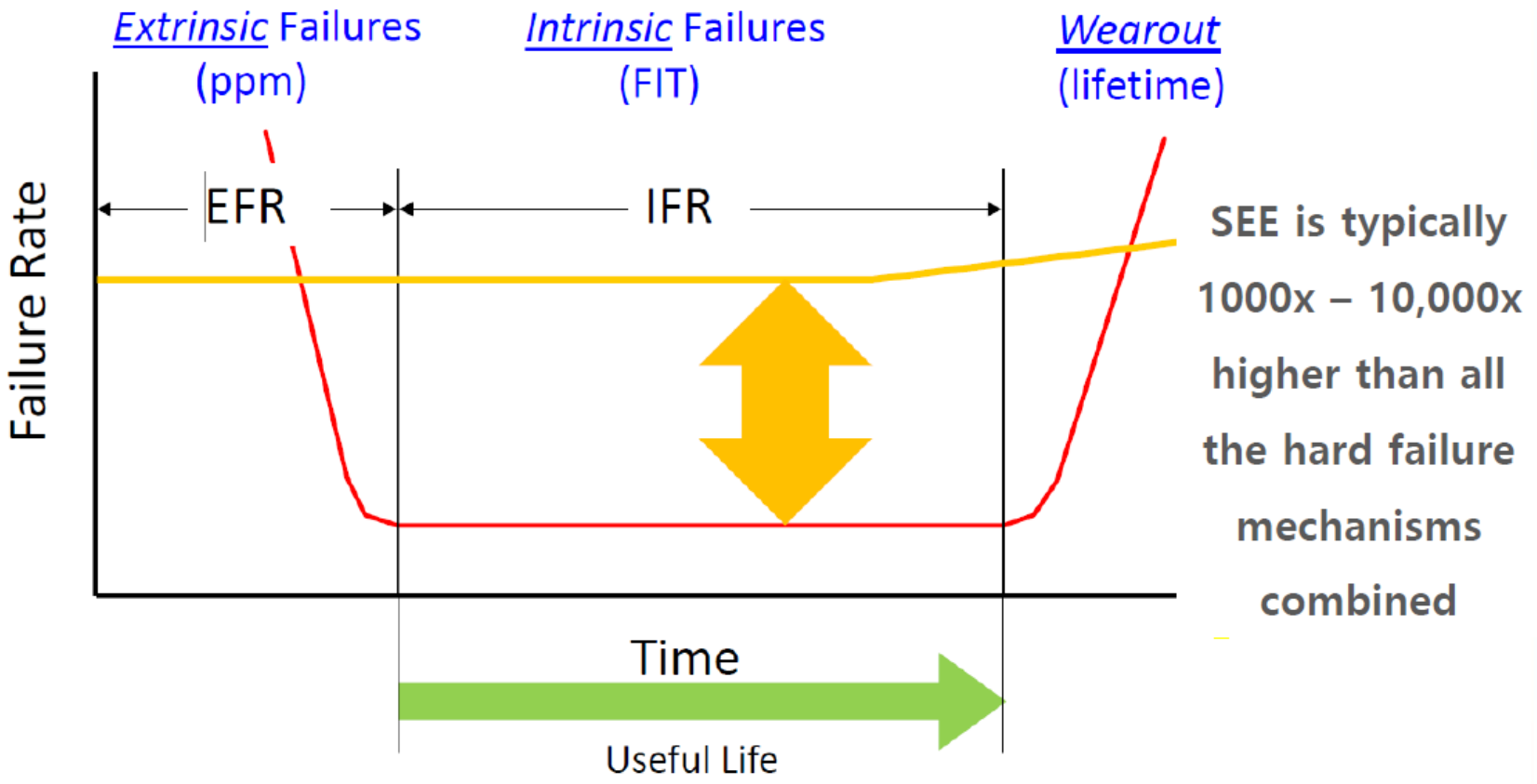
- "Soft errors have become a huge concern in advanced computer chips because, uncorrected, they produce a **failure rate exceeding that of all other reliability mechanisms combined.**"

  Baumann, Robert. "Soft errors in advanced computer systems." IEEE Design & Test of Computers 22, no. 3 (2005): 258-266.

- "Thus, one could postulate that there will be a cross-over point where **SET induced error rates will exceed the traditional SEU error-rates**"

  La Bel, Kenneth A., and Lew M. Cohn. "Radiation testing and evaluation issues for modern integrated circuits." (2005).

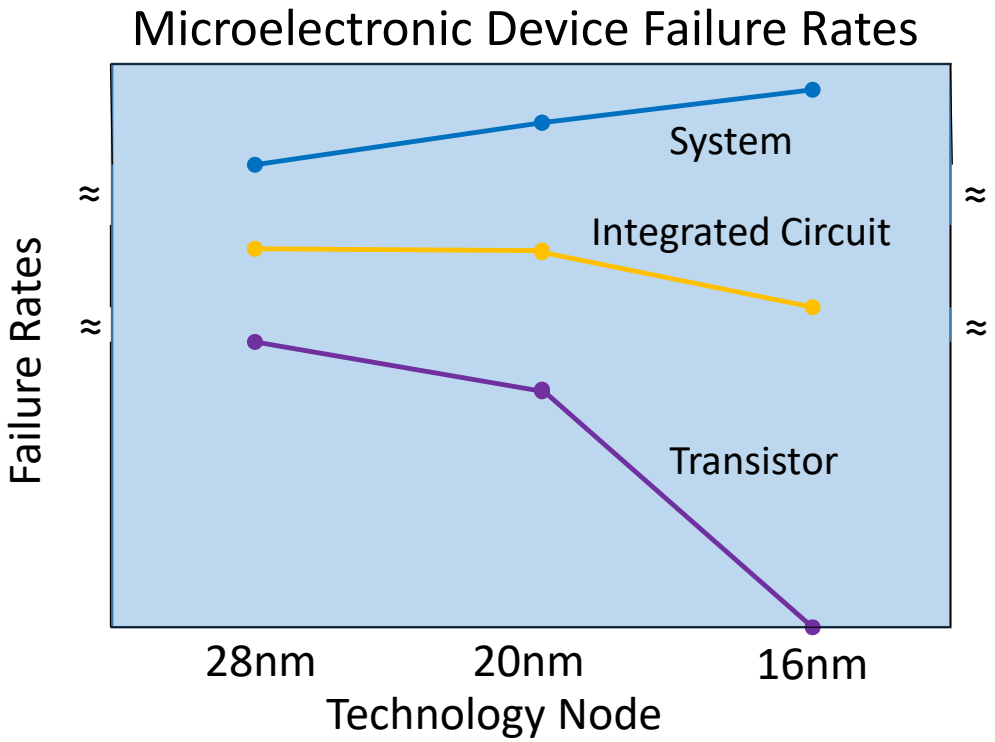
왜 Soft Error가 주목을 받고 있나?



After Robert C. Baumann, "LANDMARKS IN TERRESTRIAL SINGLE-EVENT EFFECTS" IEEE 50th *2013 NSREC Short-Course*

왜 Soft Error가 주목을 받고 있나?

Tech에 따른 SER의 변화



Bharat Bhuva – Vanderbilt University

왜 Soft Error가 주목을 받고 있나?

➢ ISO 26262 Requirements

	ASIL-B	ASIL-C	ASIL-D
Random HW Faults	<= 100 FIT	<= 100 FIT	<= 10 FIT
Single Point Fault Metric	>=90%	>=97%	>=99%
Latent Fault Metric	>= 60%	>= 60%	>= 90%

Table 1 — Properties of modular hardware design

		ASIL			
		A	B	C	D
1a	Hardware design walk-through[a]	++	++	o	o
1b	Hardware design inspection[a]	+	+	++	++
2	Safety analyses	In accordance with 7.4.3			
3a	Simulation[b]				
3b	Deve				

NOTE

[a] Methoc hardware de

[b] Methoc analytical m

Table 6 — Possible source for the derivation of the random hardware failure target values

ASIL	Random hardware failure target values
D	$<10^{-8}$ h^{-1}
C	$<10^{-7}$ h^{-1}
B	$<10^{-7}$ h^{-1}

NOTE The quantitative target values described in this table can be tailored as specified in 4.1 to fit specific uses of the item (e.g. if the item is able to violate the safety goal for durations longer than the typical use of a passenger car).

ISO 26262가 안전에 미치는 영향

- 2014년도 미국 통계에 따르면 :
  - 3026 Billions 자동차 주행 Miles 당 32,675 사망건수
- 가정 :
  - 0.02 hours/mile (i.e. 50 mph)
- 결과는 :
  - Event rate is ~500 FITs (Failure In Time – event/billion working hours)
- ISO26262의 ASIL D는 10 FITs으로 정하고 있다.
  - ~50x 배 신뢰성 이상의 개선이 요구된다
  - … 몇 %정도만 실지로 생명에 위험을 주는 사고로 이어질 수 있다
  - 실질적인 신뢰성 개선은 더 높아야 한다
- 전 세계적으로 (Statistics by Association for Safe Inter. Road Travel)
  - 일년 동안 130만 명의 인명 피해
  - 90%이상의 인명피해는 중산 수입 국가들에서 생기며, 전세계 차량의 반 이하가 운행
  - 전 세계 자동차 크래쉬 사고는 미화로 $518B 정도인데, 각 해당 국가의 일년 GDP의 1-2%

Dan Alexandrescu, "How EDA can Improve Productivity in the Assessment of Functional Safety", IOLTS 2016

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반도체 Soft Error 평가 방법

SER 평가 방법 1 : Real Time Test

LSBB: Lab. Souterrain Bas Bruit

고도 550m

IRAM Lab at Pic de Bure

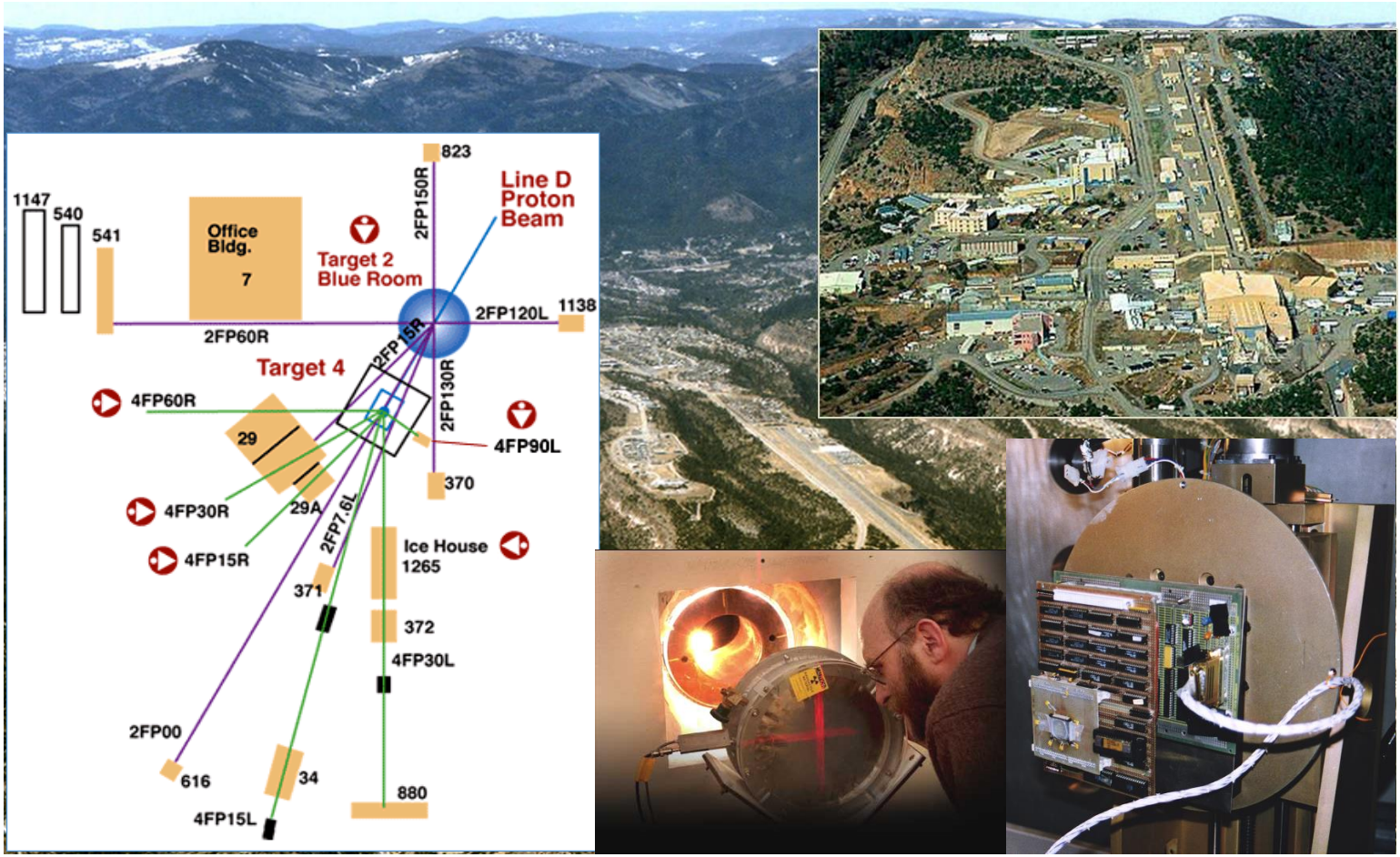
고도 2,552m

ROSETTA Project

L2MP Lab, Marseille

고도 124m

SER 평가 방법 2 : Accelerated Beam Test



LANCE Los Alamos, USA

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반도체 Soft Error에 대한 대응 방안

Soft Error 감소 방안

- Source를 차단
- Charge Collection을 최소화
- Charge 변화에 둔감하게
- Fault의 전달을 막음
- Error 발생을 감지하여 올바른 값으로 수정

- Device level
- Circuit level
- System level

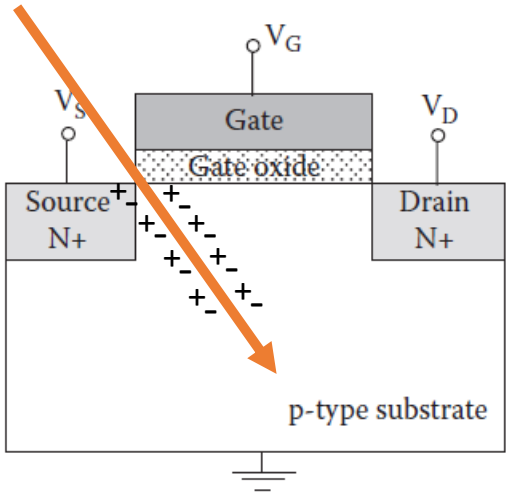
Source를 차단

- Neutron 불가능
  - 3m 이상 두께의 강화 콘크리트 필요

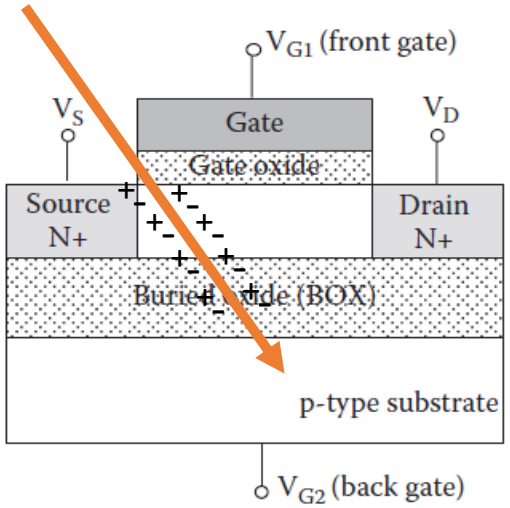
- Low alpha Material 사용
  - LA : Low Alpha <0.05 a/hr cm2
  - ULA : Ultra Low Alpha <0.002 a/hr cm2
  - SLA : Super Ultra Low Alpha <0.001 a/hr cm2

Substrate Level

- Confinement of charge collection volume
- Deep N-well
- SOI (Silicon on Insulator)

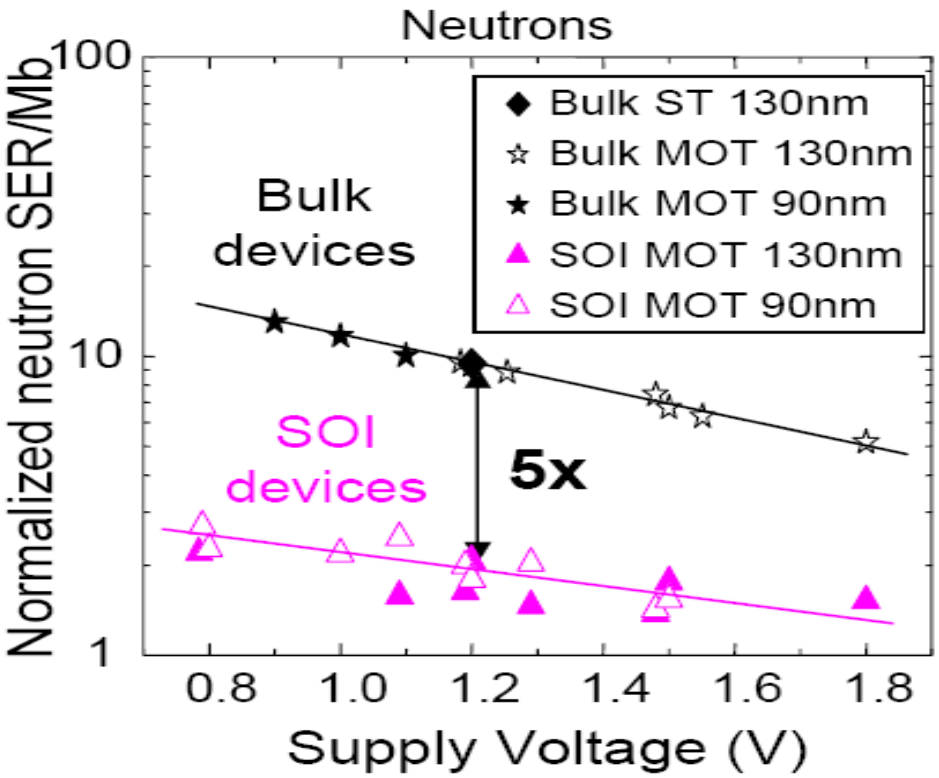


Normal MOSFET



SOI MOSFET

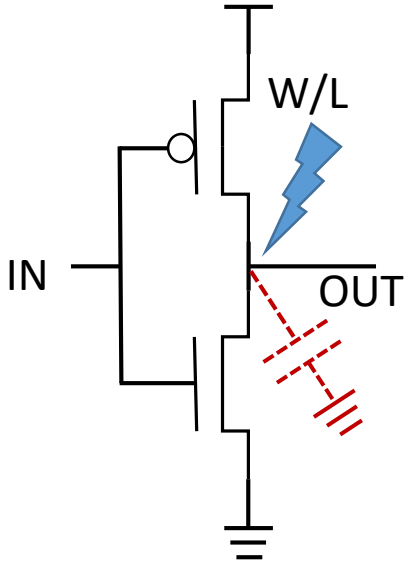
SER of SOI MOSFET Products

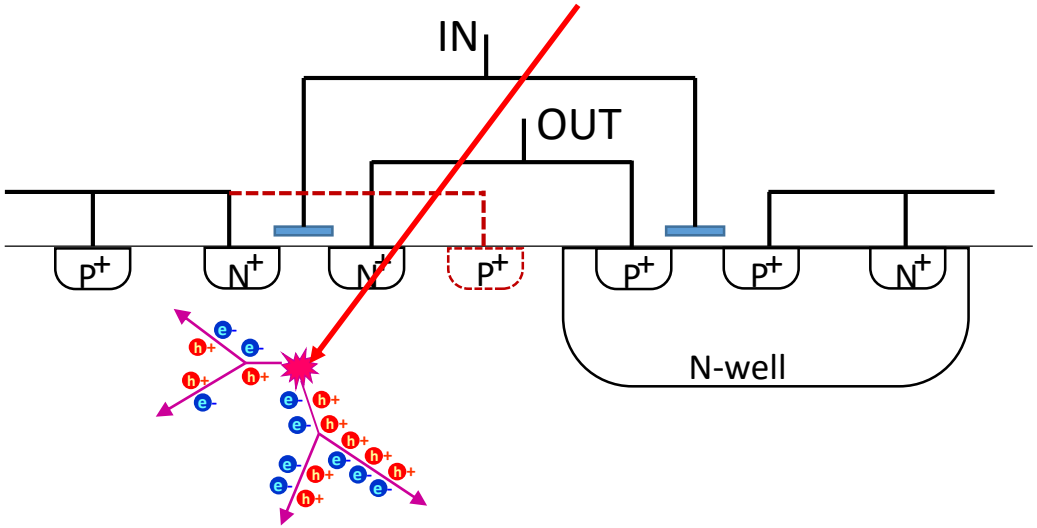


R. Baumann, 2005 NSREC Short Course

Device level

- Increasing the critical charge
  - Add capacitor to the nodes
  - Widen width of the transistors
- Add guard contact/electrode



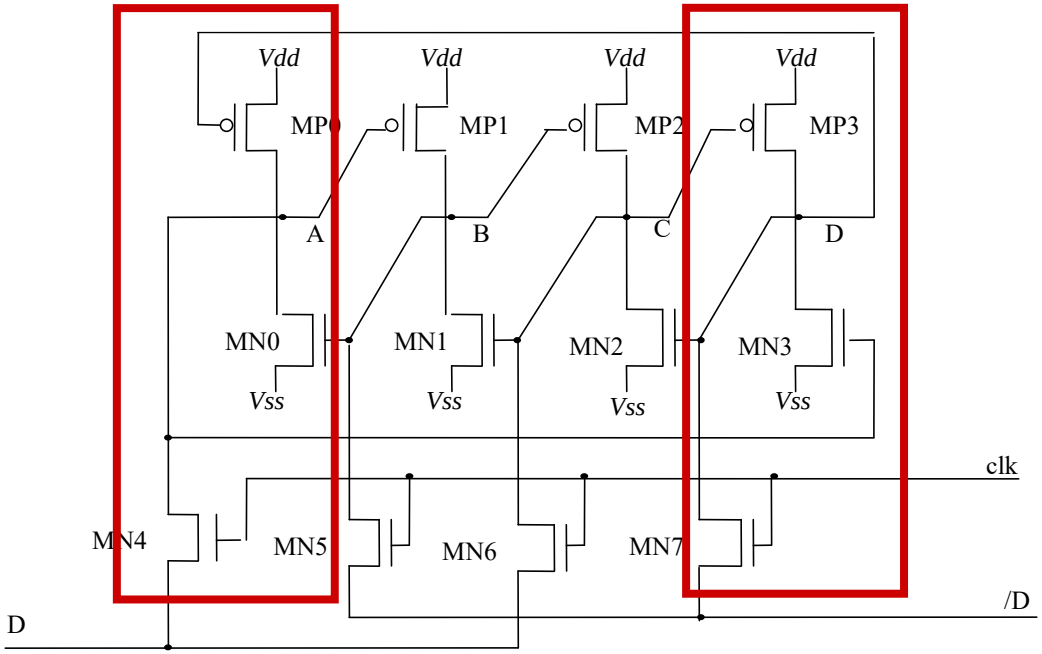


- Increased area

Circuit Level

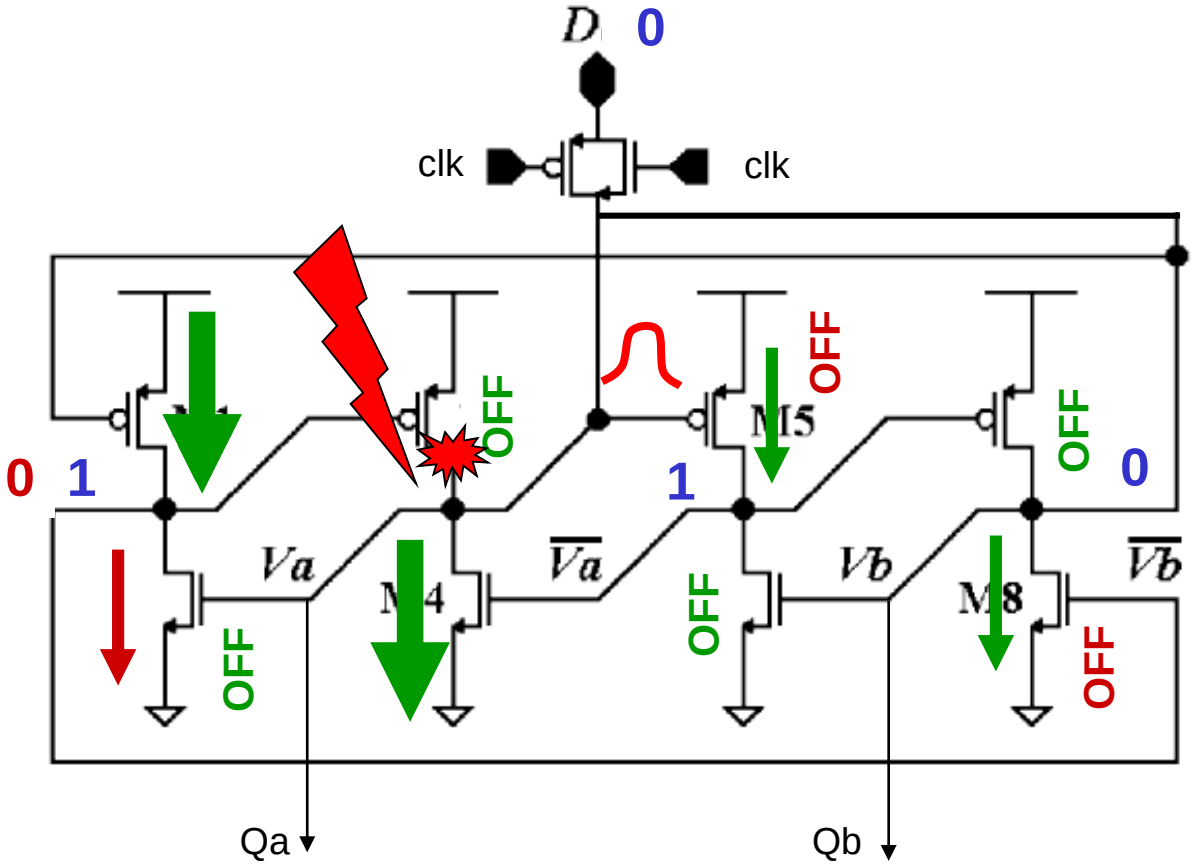
- Space Redundancy
  - To store data in two different locations in such way that the corruption can be restored
  - To have redundant task blocks and select the most popular output
- Time Redundancy
  - Instead of using redundant blocks, use several times the same block

DICE (Dual Interlocked Storage Cell)



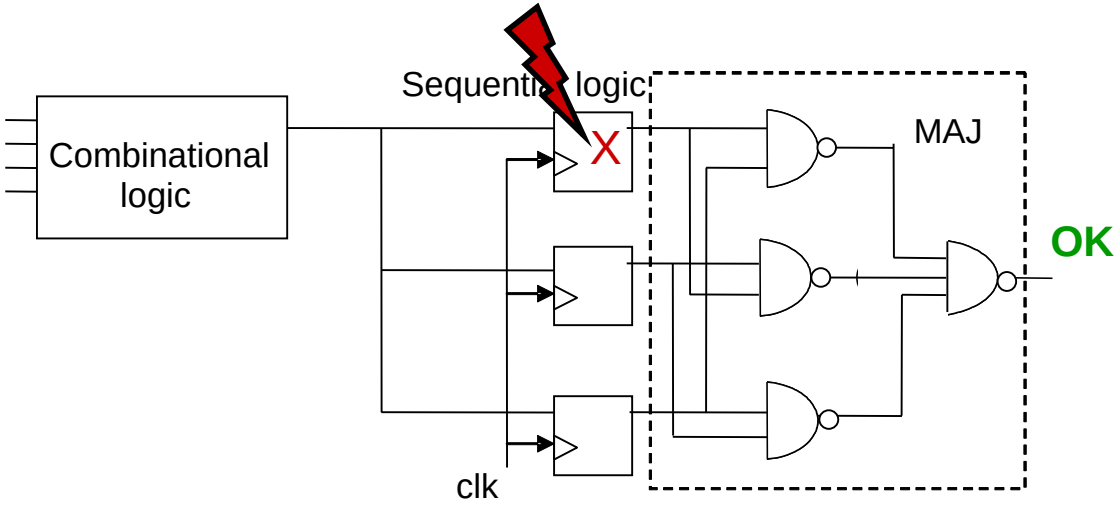
DICE Memory Cell [Calin, 96]

DICE의 동작



2배의 회로 면적이 필요

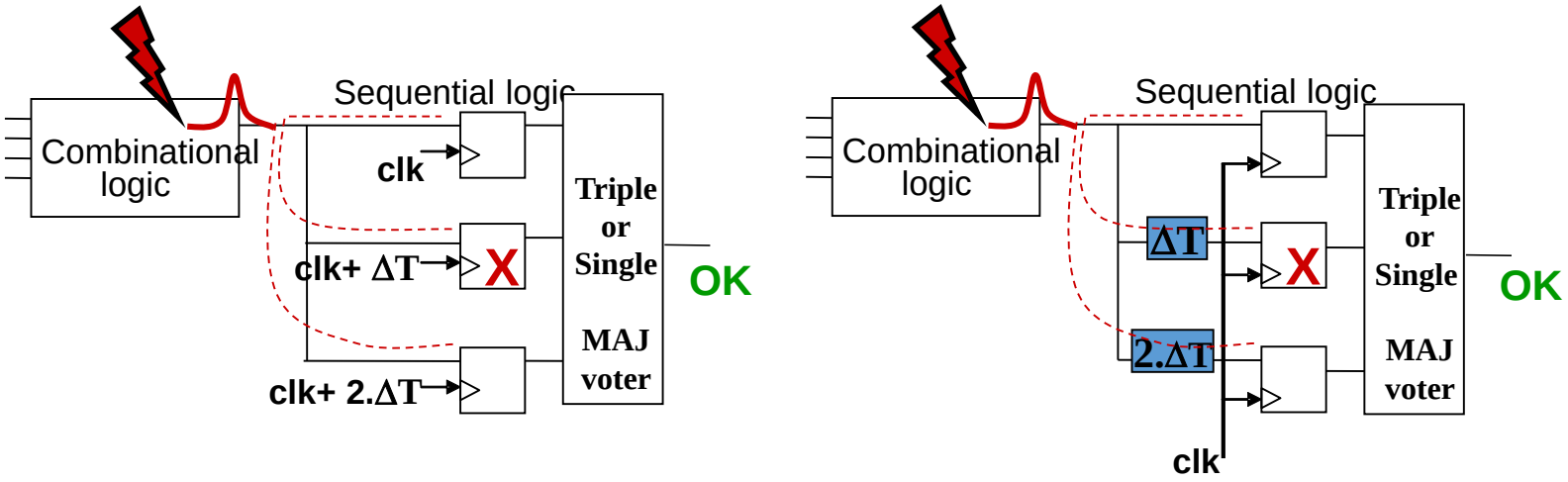
TMR(Triple Modular Redundancy)



inputs	MAJ
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1

- Easy to implement
- Area penalty
- Combinational logic 이나 Voting logic이 radiation에 노출되면 오동작

Time Redundancy Filtering

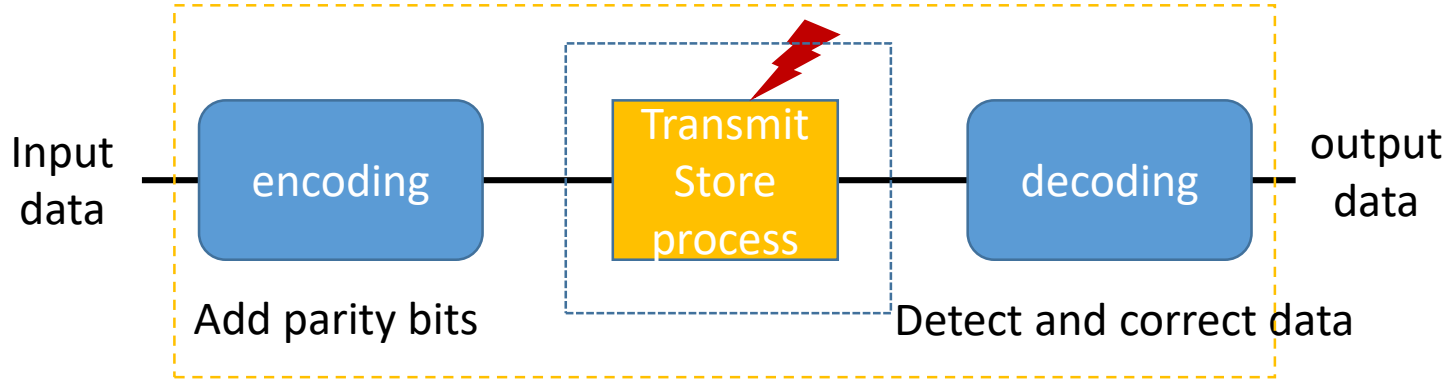


[Nicolaidis, VTS 1999], [Anghel et al., DATE 2000]

- Frequency limitations

ECC (Error Correction Code)

- Transmit after adding parity bits
- 1bit error correction
- 2bit error detection
- 4bit parity bits for 8bit data (in Hamming code)



- easy to implement
- effective memory size 감소

Software Redundancy

- Add check and correct by calculating twice, sequentially or in parallel

- Pro
  - Able to apply to any devices
  - Able to detect more than 90% of anomaly

- Con
  - Programming is not so simple
  - Size of program soars up to 3-4 times

How much mitigation is enough?

- How is it possible to know that the mitigation technique is working properly for a certain Soft Error Rate (SER)?

- It is necessary to have a mechanism to inform the system when the number of multiple faults have passed a certain level

- Built-in Self Test (BIST) Mechanism:
  - sensors working as watch dogs
  - each time an ionization occurs, the system is informed

Trade-offs

- There is always some penalty to be paid when protecting circuits against upsets.

- Each technique may present a combination of:
  - area overhead,
  - performance penalty,
  - power dissipation increase

- The challenge is to select the most cost-effective techniques for the target circuit application

Summary

- 반도체 Soft Error는 Alpha Particle이나 Neutron과 같은 고에너지 입자가 반도체와 반응하여 생긴 전하가 유발

- 반도체의 미세화, 시스템 내 반도체의 사용량 증가, 안전에 대한 요구의 강화 등으로 Soft Error의 관리가 더욱 중요해짐

- 반도체에 주입되는 입자의 양을 줄이거나 Soft Error의 발생을 줄이는 회로적, 시스템적 방안이 개발되었으나 면적이 커지거나 성능이 저하되는 단점이 있어 평가를 통해 적정 수준과 방법을 정하는 것이 중요

thank you!

Q & A